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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/043,847	01/11/2002	Raymond R. Hoare II	01-014-US	1170

7590 08/30/2005

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EXAMINER	
SAXENA, AKASH	
ART UNIT	**PAPER NUMBER**
2128	

DATE MAILED: 08/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/043,847	HOARE ET AL.	
	Examiner	Art Unit	
	Akash Saxena	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-50* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/28/02, 8/13/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-50 have been presented for examination based on the application filed on 11th January 2002.

Priority

2. Acknowledgement is made to domestic priority under 35 U.S.C. 119(e) to application 60/267529 filed on 29th February 2001.

Claim Interpretation

3. Claim 1: "IEEE 100 The Authoritative Dictionary of IEEE Standard Terms (7th Edition)" defines the discrete event model (simulation) and associated terms as follows:

> *Discrete simulation:* A simulation that uses a discrete model.
> *Discrete event model:* See: discrete model.
> *Discrete model:* (A) A mathematical or computational model whose output variables take only discrete values; that in changing from one value to another they do not take on intermediate values; for example a model that predicts an organization's inventory levels based on varying shipments and receipts. (B) A model of a system that behaves in a discrete manner.

4. Claim 11:states

> "The discrete event simulator of claim 10, wherein said pending event queue and said future event queues are conventional computer bus structures."

It is unclear to the examiner what is meant by pending and future event queues are conventional bus structures. It is interpreted as these queues are passed over on conventional buses.

Specification

5. A series of singular dependent claims is permissible in which a dependent claim refers to a preceding claim which, in turn, refers to another preceding claim.

A claim, which depends from a dependent claim, should not be separated by any claim, which does not also depend from said dependent claim. It should be kept in mind that a dependent claim may refer to any preceding independent claim. In general, applicant's sequence will not be changed. See MPEP § 608.01(n).

Claim 34 is improperly numbered and should be numbered claim 5 instead. Appropriate corrections are required.

6. Applicant is reminded of the proper language and format for an abstract of the disclosure. Current abstract is 168 words.

> The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.
>
> The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claim 11 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The phrase "...queues are conventional bus structures" is vague and examiner is unable to correlate the queue and the bus structure. Further, examiner is unclear what is meant by the bus structure with respect to queues.
8. Claim 18 recites the limitation "next event RAM". There is insufficient antecedent basis for this limitation in the claim. Specification does not disclose a "next event RAM", instead only disclose "next" RAM (Specification: Pg.66 [183]).

Appropriate corrections are required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claim 1, 7, 10, 12, 40 & 42 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,117,181 issued to Glenn A. Dearth et al (DE '181 hereafter).

Regarding Claim 1

DE '181 teaches a discrete event simulator (DE '181: Fig.2; Col.13 Line 5 – Col.14 Line 40) with an event scheduler as hub and at least one remote simulation engine communicatively connected to the hub by remote procedure calls (DE '181: Col.5 Lines 45-59; Col.6 Lines 27-32). The hub is used to control the flow of future events (DU: Col.8 Lines 18-26; Col.9 Lines 40-46) and simulation is used to evaluate the pending future events (DU: Col.8 Lines 48-56; Col. 6 Lines 62-67).

Regarding Claim 7

DE '181 teaches a discrete event simulator with more than one simulation engine, wherein each simulation engine is directly connected to the event scheduler (hub) (DE '181: Fig.1, Elements 140A-140C; Fig.2, Elements 140A, 260).

Regarding Claim 10

DE '181 teaches discrete event simulator comprising pending events queue directly connecting to the scheduler to a simulation engine. DE '181 teaches that the user thread (containing the pending event) can initiate transaction with the simulation system through the use of mailbox in the simulation system this synchronization & data transfer however happens through the scheduler (hub) (DE '181: Col.8 Lines 48-56; Col.6 Lines 62-67). This detail is present in a copending by also by same inventor (Now Patent No. 5,732,247 (**DE '247** hereafter)), which is incorporate by reference by DE '181 (DE '181: Col.8 Lines 55-56, Col.1 Lines 13-19).

DE '247 teaches that test core communicates with the scheduler/common interface core/hub (DE '247: Fig.1 Element 11(1), 26, 20, 24, 13(1)), which directly connects to the simulation engine (Element 13(1)). Further, DE '181 teaches future event queue connecting the simulation engine to the scheduler/hub (Col.9 Lines 25-56).

Regarding Claim 12

DE teaches the pending & future queues as shown above and show they are connected from point-to-point between the scheduler and the simulation engine through the appropriate interface (DE: Fig.2 Element 130, 140A).

Regarding Claim 40

Claim 40 discloses similar limitations as claim 1 and is rejected for the same reason as claim 1.

Regarding Claim 42

Claim 42 discloses similar limitations as claim 7 and is rejected for the same reason as claim 7.

10. Claims 2 is rejected under 35 U.S.C. 102(e) as anticipated by DE '181 or, in the alternative, under 35 U.S.C. 103(a) as obvious over U.S. Patent No. 6,026,230 issued to Lin et al (LI hereafter).

Regarding Claim 2

DE '181 teaches at least one simulation engine (DE '181: Fig.2 Elements 140A; Fig.1 Elements 140A-C) with a model core (DE '181: Fig.2 Element 260), where the model core can specify in HDL a portion of the simulated circuit (DE '181: Col.6 Lines 27-28).

If the model cores in the claim 2 are interpreted as "consisting" of all the components (truth table, lookup etc...), DE '181 anticipates such a model cores because all the model cores are discrete models which can be discretely implemented in the HDL in various distributed models as disclosed above.

If the claim 2 is interpreted in alternative as "model core selected from the group" comprising "of a truth table, lookup table, a reduction to finite conclusion of a continuous or transient equation, a reprogrammable core processor, a software emulated core within the model" OR "a hardware emulated core", then LI teaches specifically use of lookup table, a reprogrammable core processor (LI: Col.12 Lines 33-44). Further, LI teaches software emulated core as well as hardware-emulated cores (LI: Abstract 1-3; Col.3 Lines 44-67; Col.4 Lines 8-31) for simulation.

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of LI and apply them to DE '181 to create a distributed discrete event simulation. The motivation would have been that LI teaches that combining the hardware under software simulation control can speed up the simulation (LI: Col.3 Lines 58-67). Further, like DE '181, LI also teaches using a single scheduler to control multiple user and simulation CPU interfaces to either perform software based simulation or a hardware/programmable core based emulation (LI: Fig 45-46).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

11. Claims 3-6, 8-9, 11, 31-34, 35-37, 41, 43 & 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,117,181 issued to Glenn A. Dearth et al (DE '181 hereafter, in view of U.S. Patent No. 6,026,230 issued to Lin et al (LI hereafter).

Regarding Claim 3

Teachings of DE '181 are disclosed in the claim 1 rejection above.

DE '181 does not specifically teach logic simulation engine although DE '181 does teach simulating the HDL model cores.

LI teaches a logic-simulation engine, which simulates the structure & function specified by the HDL (LI: Col.5 Lines 8-18).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of LI and apply them to DE '181 to create a distributed discrete event simulation. The motivation would have been that LI teaches that combining the hardware under software simulation control can speed up the simulation (LI: Col.3 Lines 58-67). Further, like DE '181, LI also teaches using a single scheduler to control multiple user and simulation CPU interfaces to either perform software based simulation or a hardware/programmable core based emulation (LI: Fig 45-46).

Regarding Claim 4

LI teaches a simulation engine comprising a memory simulation engine (LI: Col.6 Lines 57 – Col.7 Lines 4).

Regarding Claim 5

LI teaches a simulation engine comprising a software simulation engine (LI: Col.4 Lines 8-10).

Regarding Claim 6

LI teaches a simulation engine comprising an interconnect simulation engine to fine-tune the delay simulation when the design is spread out on a reprogrammable c ore processor (LI: Col.26 Lines 50-67).

Regarding Claim 8

DE '181 teaches simulation engines but is not specific on various purposes (logic, memory, software and interconnect) of simulation (Fig.2, Elements 140A) as claimed, although DE '181 anticipates all of them. LI teaches a simulation engine selected from the group of containing logic simulation engine (LI: Col.5 Lines 8-18), a memory engine LI: Col.6 Lines 57 – Col.7 Lines 4), a software engine (LI: Col.4 Lines 8-10), interconnect engine (LI: Col.26 Lines 50-67).

Regarding Claim 9

LI teaches that simulation engines (systems) can be of same type (LI: Col.5 Lines 3-4).

Regarding Claim 11

DE '181 teaches a scheduler with pending and future event queues in claim 10 above. LI teaches that the scheduler can be connected to the simulation engine (LI: Fig.46, Elements 1117, 13, 50, 7) though conventional bus (PCI bus disclosed).

Regarding Claim 31

DE '181 does not teach host workstation for controllability and observability of the simulation explicitly, although his motivation for his design is both controllability and observability (DE '181: Col.6 Lines 33-45; 45-53 (observe); 54-61 (control)).

LI teaches a host workstation communicatively coupled to the event scheduler and simulation engine explicitly (LI: Fig.46 Elements 1111-1113, 1117, 1119-1120, 61 & 70).

Regarding Claim 32 & 33

LI also teaches that simulation setup can be altered at runtime analysis can be performed (LI: Col.3 Lines 58-Col.4 Lines 7).

Regarding Claim 34

LI teaches that memory simulation engine comprises of data storage RAM (LI: Col.7 Lines 37-43), emulation logic (LI: Col.7 Line 635-17) and configuration RAM (Col.6 Lines 57-63).

Regarding Claim 35

LI teaches universal device primitives representing the elements being simulated (LI: Col.22 Lines 47-52).

Regarding Claim 36

Claim 36 discloses similar limitation as claims 1, 10 and 31 combined and is rejected for the same reasons as claims 1, 10 and 31.

Regarding Claim 37

Claim 37 discloses similar limitations as claim 2 and is rejected for the same reason as claim 2.

Regarding Claim 41

Claim 41 discloses similar limitations as claim 31 and is rejected for the same reason as claim 31.

Regarding Claim 43

Claim 43 discloses similar limitations as claim 8 and is rejected for the same reason as claim 8.

Regarding Claim 45

Claim 45 discloses similar limitations as claim 35 and is rejected for the same reason as claim 35.

12. **Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,117,181 issued to Glenn A. Dearth et al (DE '181 hereafter, in view of IEE article "XPOSE: A Simulator for Network Development" by Deborra Zukowski at al (ZU 1994 hereafter).**

Regarding Claim 13

Teachings of DE '181 are disclosed in the claim 12 rejection above. DE '181 discloses that point-to-point connections between simulation engine and the scheduler can be made through the network (DE '181: Col.4 Lines 54-65).

DE '181 does not specifically teach gigabit conduits to make point-to-point connections between simulation engine and the scheduler.

ZU 1994 teaches that network simulation for architectural and functional verification done in VHDL can be performed using gigabit network (ZU 1994: Abstract; Pg 59 Col. 2 ¶ 2).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of ZU 1994 and apply them to DE '181 to create a distributed gigabit network point to point simulation. The motivation to combine would have been that ZU 1994 teaches that gigabit network simulation can provide hardware/software co-simulation using VHDL (ZU 1994: Pg.67 Col.1 "Conclusion").

13. Claims 14-16, 18, 21-22, 38-39, 44, 46 & 47-48 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,117,181 issued to Glenn A. Dearth et al (DE '181 hereafter), in view of U.S. Patent No. 5,914,934 issued to Rathnavelu (RA hereafter).

Regarding Claim 14

Teachings of DE '181 are disclosed in the claim 1 rejection above. DE '181 has a concept of timing wheel and synchronization events but does not detail them explicitly (DE '181: Col.13 Lines 6-16)

DE '181 does not explicitly teach a timing wheel.

RA teaches use of timing wheel in a system requiring scheduling based on time (RA: Col.2 Lines 47-50).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of RA with DE '181 to make a scheduling system in which each event is associated to a time in at least one timing wheel. The motivation to combine would have been that RA is solving the problem of scheduling based on timing with multiple incoming (pending events) and outgoing (future) queues based on latency (RA: Col.2 Lines 32-46). DE '181 encounters this problem of scheduling on an event basis, time basis from various simulation engines and tests (DE '181: Fig 2).

Regarding Claim 15

RA also teaches that is possible to have multiple timing wheels to accommodate multiple granularity of wheels (defined as class of wheels based on latency of required) (RA: Col.3 Lines 17-20).

Regarding Claim 16

RA teaches that the scheduler comprises of an event RAM for holding queue of received events as the pending queue (RA: Fig.1 Elements 16 & 17; Col.1 Lines 54-56, 65-66). Further, RA teaches the scheduler comprises a pointer RAM for holding head of queue pointers, which point to the first element in a queue of events for each simulation time period (RA: Fig.1; Fig.2; Col.3 Lines 56-58; Col. 4 Lines 46-55).

Regarding Claim 18

RA teaches that the event RAM (VC table in memory) includes a data RAM to store the incoming event in the pending queue and a next event RAM pointing to the next event (RA: Col.3 Lines 61-64).

Regarding Claim 21

DE '181 teaches a local synchronization thread (LST) and barrier mechanism which controls the release of the pending events to the simulation system (DE '181: Abstract). Since the LST thread is implemented in memory of the scheduler (hub), rollover functionality to reuse the released LST space would be necessitated by limited memory space available. Further RA also is concerned with the cluster size and marking the cluster (event RAM) empty; hence implements the claimed rollover functionality (RA: Col.5 Lines 6-36).

Regarding Claim 22

DE '181 teaches the global synchronization (virtual) time to keep track of the simulation time of various simulations and synchronizes them, whereby releasing the pending events at one time though the disclosed barrier (DE '181: Col.13 Lines 6 – 27; Abstract).

Regarding Claim 38

Claim 38 discloses similar limitations as claim 16 and is rejected for the same reason as claim 16.

Regarding Claim 39

Claim 39 discloses similar limitations as claim 18 and is rejected for the same reason as claim 18.

Regarding Claim 44

Claim 44 discloses similar limitations as claim 16 and is rejected for the same reason as claim 16.

Regarding Claim 46

Claim 46 discloses similar limitations as claim 16 and is rejected for the same reason as claim 16.

Regarding Claims 47 & 48

Claims 47 & 48 discloses similar limitations as claim 22 and are rejected for the same reason as claim 22.

14. Claims 17, 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,117,181 issued to Glenn A. Dearth et al (DE '181 hereafter), in view of U.S. Patent No. 5,914,934 issued to Rathnavelu (RA hereafter), further in view of U.S. Patent No. 6,088,760 issues to Walker et al (WA hereafter).

Regarding Claims 17, 19 & 20

Teachings of DE '181 & RA are disclosed in the claim 16 rejection above.

DE '181 teaches memory (RAM) used to store and run simulation (DE '181: Fig.2).

RA also teaches use of memory array to making up the pointer RAM (RA: Col.3 lines 55-58).

DE '181 and RA do not teach dual ported RAM. Further, they do not teach read/write on one clock cycle and RAM being 144 bits wide.

WA teaches multi-ported (two ports displayed) ported RAM (WA: Col.2 Lines 58-61; Fig.1) with one clock cycle read/write capability (WA: Col.6 Lines 17-26) and storage, which is 256 bits wide (larger than the claimed 144 bits, hence can accommodate 144 bits wide data storage) (WA: Fig.1 Element 12).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of WA to DE '181 and RA to create a dual ported fast RAM. The motivation to combine would have been that the wider dual ported RAM memories allow concurrent data read and write without the need for providing the address data for subsequent memory accesses and also reducing the pin requirements (WA: Col.9 Lines 10-24).

15. Claims 23-25, 27-30 & 49-50 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,117,181 issued to Glenn A. Dearth et al (DE '181 hereafter, in view of U.S. Patent No. 4,787,061 issued to Nei et al (NE hereafter).

Regarding Claim 23

Teachings of DE '181 are disclosed in the claim 1 rejection above. DE '181 teaches a simulation engine as disclosed above.

DE '181 does not teach a simulation engine comprising a pipelined structure such that incoming events can be evaluated at each clock cycle.

NE teaches a pipelined simulation engine which can process the incoming events at each clock cycle (NE: Abstract; Col.3 Lines 53-58).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of NE to DE '181 to use a pipelined simulation engine. DE '181 teaches a local synchronization thread (LST) and barrier mechanism which controls the release of the pending events to the simulation system (DE '181: Abstract). The motivation to combine would have been that multiple events could have been released to the simulation engine (interface) (DE '181: Fig.1 Element 262) and need accelerated processing when they are released from the LST (DE '181: Fig.1 Element 208B) interface.

Regarding Claim 24

NE teaches a simulation engine adapted to simulate the intrinsic delay within each structure being simulated with unit delay (NE: Col.3 Lines 21-30; Col.1 Lines 56-65) and/or multiunit delay (NE: Abstract) using the time-wheel mechanism.

Regarding Claim 25

NE teaches a simulation engine adapted to simulate the extrinsic delay due to output load for each structure being simulated by using the fan-out calculation using the circuit netlist (NE: Col.4 Lines 27-33).

Regarding Claim 27

NE teaches a netlist engine in the simulator which is capable of generating additional events that account for the capacitive load due to fanout from the first discrete event element and leads to evaluation of nets based on fanout and delay calculation (NE: Col.3 Line 53 – Col.5 Line 37).

Regarding Claims 28, 29 & 30

NE teaches the netlist engine, which is part of the timing & functional simulation engine (Col.1 Lines 48-52, 56-58). Regarding placement of the netlist engine, DE '181 teaches that the scheduler (hub) could have other simulation running in parallel (DE '181: Fig.1 Elements 140 A-C) to net list simulation. Further claims relating to the netlist simulation engine being before or after the simulation are both covered in the NE reference (NE: Col.3 Line 53 – Col.5 Line 37; Fig.1).

Regarding Claims 49 & 50

Claims 49 & 50 discloses similar limitations as claim 27 and are rejected for the same reason as claim 2.

16. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,117,181 issued to Glenn A. Dearth et al (DE '181 hereafter, in view of U.S. Patent No. 5,655,107 issued to Michael Bull (BU hereafter).

Regarding Claim 26

Teachings of DE '181 are disclosed in the claim 1 rejection above. DE '181 teaches a simulation engine as disclosed above.

DE '181 does not teach the simulation engine to simulate the wire delay simulation between each structures being simulated.

BU teaches a simulation engine with ability to calculate the wire delay based on the net interconnection (BU: Col.2 Lines 20-42).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of BU to DE '181 to perform wire delay simulation on a distributed system. The motivation to combine would have been that the scheduler and the queuing mechanism disclosed (BU: Fig.2 Elements 30, 32) would fit in perfectly in the distributed architecture disclosed by DE '181 (DE '181: Fig.2).

Conclusion

17. All claims are rejected.

18. **Examiner's Note:** Examiner has cited particular columns and line numbers in the references applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in their entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

In the case of amending the claimed invention, Applicant is respectfully requested to indicate the portion(s) of the specification which dictate(s) the structure relied on for proper interpretation and also to verify and ascertain the metes and bounds of the claimed invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Akash Saxena whose telephone number is (571) 272-8351. The examiner can normally be reached on 8:30 - 5:00 PM M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jean R. Homere can be reached on (571)272-3780. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Akash Saxena
Patent Examiner GAU 2128
(571) 272-8351
Tuesday, August 02, 2005

Fred Ferris, GAU 2128